The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of fabricating an integrated circuit device comprising:

forming a conductive layer on a microelectronic substrate;

forming [an] a first insulating layer on the conductive layer, the first insulating layer including an overhanging portion that extends beyond the conductive layer; ~~and~~

forming a second insulating layer on the microelectronic substrate to cover the first insulating layer; and

etching the second insulting layer to form ~~forming~~ a sidewall insulating region disposed laterally adjacent a sidewall of the conductive layer and extending between the overhanging portion of the first insulating layer and the microelectronic substrate.

2. (Currently Amended) [A] The method according to Claim 1, further comprising:

forming an insulating region between the overhanging portion of the first insulating layer and the microelectronic substrate; and

forming a sidewall spacer conforming to a sidewall of the first insulating layer, the sidewall insulating region and an adjoining surface of the insulating region.

3. (Currently Amended) [A] The method according to Claim 1, wherein forming the conductive layer comprises forming the conductive layer by adjusting ~~the~~ an etchant so that the first insulating layer includes the overhanging portion that extends beyond the conductive layer.

4. (Currently Amended) [A] The method according to Claim 1, wherein forming the conductive layer comprises forming a conductive layer having first and second metallic layers.

5. (Currently Amended) A method of fabricating a self-aligned contact structure for a microelectronic device, the ~~structure~~ method comprising:

forming a conductive layer on a microelectronic substrate;

forming [an] a first insulating layer on the conductive layer, the first insulating layer including an overhanging portion that extends beyond the conductive layer;

forming a second insulating layer on the microelectronic substrate to cover the first insulating layer;

etching the second insulating layer to form [forming] a sidewall insulating region disposed laterally adjacent a sidewall of the conductive layer and extending between the overhanging portion of the first insulating layer and the microelectronic substrate; and

forming a conductive region disposed laterally adjacent to the sidewall insulating region such that the sidewall insulating region separates the sidewall of the conductive layer and the conductive region.

6. (Currently Amended) [A] The method according to Claim 5, further comprising:

forming an insulating region between the overhanging portion of the first insulating layer and the microelectronic substrate; and

forming an insulating sidewall spacer conforming to a sidewall of the first insulating layer, the sidewall insulating region and an adjoining surface of the insulating region, wherein the conductive region is laterally adjacent to the insulating sidewall spacer.

7. (Currently Amended) [A] The method according to Claim 5, wherein forming the conductive layer comprises forming the conductive layer by adjusting [the] an etchant so that the first insulating layer includes the overhanging portion that extends beyond the conductive layer.

8. (Currently Amended) [A] The method according to Claim 5, wherein forming the conductive layer comprises forming a conductive layer having first and second metallic layers.

9. (Currently Amended) A method of fabricating an integrated circuit memory device, comprising:

forming a first bit line comprising:

forming a first conductive layer on a microelectronic substrate; and

forming a first insulating layer on the first conductive layer, the first insulating layer including a first overhanging portion that extends beyond the first conductive layer; and

~~forming a first sidewall insulating region disposed laterally adjacent a first sidewall of the first conductive layer and extending between the first overhanging portion of the first insulating layer and the microelectronic substrate; and~~

forming a second bit line comprising:

forming a second conductive layer on [a] the microelectronic substrate; and

forming a second insulating layer on the second conductive layer, the second insulating layer including a second overhanging portion that extends beyond the second conductive layer; ~~and~~

~~forming a second sidewall insulating region disposed laterally adjacent a second sidewall of the second conductive layers and extending between the second overhanging portion of the second insulating layer and the microelectronic substrate~~

forming a third insulating layer on the microelectronic substrate to cover the first and second bit lines; and

etching the third insulating layer to simultaneously form a first sidewall insulating layer region disposed laterally adjacent to a first sidewall of the first conductive layer, and a second sidewall insulating region disposed laterally adjacent to a second sidewall of the second conductive layer, wherein the first sidewall insulating region extends between the first overhanging portion of the first insulating layer and the microelectronic substrate, and the second sidewall insulating region extends between the second overhanging portion of the second insulating layer and the microelectronic substrate.

10. (Currently Amended) [A] The method according to Claim 9:

wherein [the] forming the first bit line further comprises:

forming a first insulating region disposed between the first overhanging portion of the first insulating layer and the microelectronic substrate; and

forming a first sidewall spacer conforming to a sidewall of the first insulating layer, the first sidewall insulating region and an adjoining surface of the first insulating region; and

wherein forming the second bit line further comprises:

forming a second insulating region disposed between the second overhanging portion of the second insulating layer and the microelectronic substrate; and

forming a second sidewall spacer conforming to a sidewall of the second insulating layer, the second sidewall insulating region and an adjoining surface of the second insulating region.

11. (Currently Amended) [A] The method according to Claim 9:

wherein forming the first conductive layer comprises forming the first conductive layer by adjusting ~~the~~ an etchant so that the first insulating layer includes the first overhanging portion that extends beyond the first conductive layer; and

wherein forming the second conductive layer comprises forming the second conductive layer by adjusting ~~the~~ an etchant so that the second insulating layer includes the second overhanging portion that extends beyond the second conductive layer.

12. (Currently Amended) [A] The method according to Claim 9:

wherein forming the first conductive layer comprises forming the first conductive layer having first and second metallic layers; and

wherein forming the second conductive layer comprises forming the second conductive layer having third and fourth metallic layers.

13. (New) The method according to Claim 1, wherein the first insulating layer comprises a silicon oxide based material and wherein the second insulating layer comprises a silicon nitride based material or a composite of the silicon nitride based material and the silicon oxide based material.

14. (New) The method according to Claim 2, wherein the spacer comprises a

silicon nitride based material, a silicon oxide based material or a composite of silicon nitride based material and silicon oxide based material.

15. (New) The method according to Claim 4, wherein the first metallic layer comprises titanium and titanium nitride and the second metallic layer comprises tungsten.

16. (New) The method according to Claim 9, wherein forming the third insulating layer comprises planarizing the third insulating layer until the first bit line and the second bit line are exposed.

17. (New) The method according to Claim 16, wherein the third insulating layer is planarized by a chemical mechanical polishing process.